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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,386	09/28/2001	Len Schultz	42390P5728	5088

8791 7590 11/19/2004

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,386	SCHULTZ ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed August 20, 2004 in application 10/144,940.

2. Claims 1-20 are again presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-2, 4-5, 7-8, 10-11 are again rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's admitted prior art (US 2003/0074601 A1 hereafter referred to as Prior Arts).

This rejection is being applied for the same reasons set forth in the previous Office Action paper number 5, paragraphs 2-3 mailed June 03, 2004.
As per claims 1-20 see the previous office action for the teaching of Prior Arts or Klecka.

Applicant asserts that Prior Arts failed to teach or suggest the following:

4.1 In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific instructions' is used to means a unit or more instructions that depend on the specific architecture or implementation of the processor to function correctly";

4.2 the use of processor implementation-specific instructions.

Examiner respectfully transverses Applicant's argument as follows:

4.1 First, It is not true that Prior Arts failed to teach the method of correcting a machine check error as claimed by Applicant. Examiner again would like to bring Applicant attention to Prior Arts's sections [0001-0003] that addressed explicitly:

- system error detection, containment, and recovery elements of a highly reliable and fault tolerant computing environment;

- a predefined instruction address called an interrupt vector;

- storing the state of the processor at the time the interrupt generated;

- resuming execution program;

- maintaining system integrity.

Second, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific instructions' **is used to means a unit or more instructions that depend on the specific architecture or implementation of the processor to function correctly**) is not recited in the rejected claims. Although the claim is interpreted in light of the specification, limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)*.

Third, Prior Arts explicitly teaches processor and software/hardware necessary to support the processor operation. Prior Arts further addresses the maintaining system integrity depends upon coordination and cooperation between the system

CPUs, platform hardware fabric, and the system software (i.e., architecture).

It is clearly that Prior Arts's error detection and correction capabilities do explicitly teach the Applicant's invention.

4.2 First, It is not true that Prior Arts failed to teach the "use of processor implementation-specific instructions" as claimed by Applicant. Examiner again would like to bring Applicant attention to Prior Arts's sections [0001-0002] that addressed explicitly to 1) processor and software/hardware necessary to support the processor operation and 2) a predefined instruction address in supporting the error detection and correction method.

This is clearly shown that Prior Art does implement the processor specific instructions therein to ensure the system operated in free of failure.

Second, Prior Arts explicitly teaches processor and software/hardware necessary to support the processor operation. Prior Arts further addresses the maintaining system integrity

depends upon coordination and cooperation between the system CPUs, platform hardware fabric, and the system software.

It is clearly that Prior Arts's error detection and correction capabilities do explicitly teach the Applicant's use of processor implementation-specific instructions.

5. Claims 1-20 are rejected under 35 U.S.C. § 102(e) as being unpatentable Klecka et al. (US Patent 6,393,582 hereafter referred to as Klecka).

Applicant asserts that Klecka failed to teach or suggest the following:

5.1 In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific instructions' is used to means a unit or more instructions that depend on the specific architecture or implementation of the processor to function correctly";

5.2 the use of processor implementation-specific instructions.

Examiner respectfully transverses Applicant's argument as follows:

5.1 First, It is not true that Klecka failed to teach the method of correcting a machine check error as claimed by Applicant. Examiner again would like to bring Applicant attention to Klecka's error checking and recovery using processor architecture [abstract, fig. 1] that addressed explicitly:

- data processing architecture [col. 1, lines 5-7];
- processor execution of instruction by instruction and instruction streams [col. 1, lines 55-56];;
- storing the state of the processor [col. 1, lines 66-67];
- error detection and correction capability [col. 1, lines 61-64];
- resuming operation based on error detection and correction recovery [col. 2, lines 1-3].

Second, in response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the feature upon which Applicant relies (i.e., In paragraph [0013] of the specification as filed applicant stated, "The term 'processor implementation-specific

instructions' **is used to means a unit or more instructions that depend on the specific architecture or implementation of the processor to function correctly**) is not recited in the rejected claims. Although the claim is interpreted in light of the specification, limitations from the specification is not read into the claims. *In re Van Guens, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)*.

Third, Klecka explicitly teaches the "inter-processor communication in a multiple processor system including I/O communication between logical processor and various peripheral computing devices [col. 3, lines 5-27] in supporting the error checking and recovery process. Klecka further illustrates four error detection and correction scenarios therein [col. 6, lines 37 through col. 8, line 49] among processors and their processor implementation-specific instructions. This is clearly shown that Klecka does teach "a unit or more instructions that depend on the specific architecture or implementation of the processor to function correctly" as claimed by Applicant.

5.2 It is not true that Klecka failed to teach the "use of processor implementation-specific instructions" as claimed by Applicant. Examiner again would like to bring Applicant

attention to Klecka's master and shadow processor units or architecture execution per their instruction stream in supporting the fault tolerant system operation [col. 10, lines 12-16]. Klecka further emphasizes the use of processor implement-specific instruction via the instruction stream including the error detection and correction means, saving processor state and data in memory, resetting processors, and resuming processors operation [col. 12, lines 39-51].

This is clearly shown that Klecka does implement the processor specific instructions therein to ensure the system operated in free of failure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML
11/10/04